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Please replace the paragraph beginning at page 62, line 16, through page 63, line 2, with the following rewritten paragraph:

The same applies to cases in which the source driver circuit 14 is formed on the array board 71 by polysilicon technology such as low-temperature polysilicon technology. A plurality of inverter circuits are formed between an analog switching gate such as a transfer gate which drives the source signal line 18 and the shift register of the source driver circuit 14. The following matters (shift register output and output stages which drive signal lines (inverter circuits placed between output stages such as output gates or transfer ~~gates)~~ gates)) are common to the gate driver circuit and source driver circuit.

Please replace the paragraph beginning at page 64, line 24, through page 65, line 7, with the following rewritten paragraph:

When the display panel is used for information display apparatus such as a cell phone, it is preferable to mount (form) the source driver IC (circuit) 14 and gate driver IC (circuit) 12 on one side of the display panel as shown in Figure 9 (incidentally, a configuration in which driver ICs (circuits) are mounted (formed) on one side of a display panel is referred to as a three-side free configuration (structure). Conventionally, the gate driver IC 12 is mounted on an X side of a display area and a source driver IC 14 is mounted on a Y side). This makes it easy in the design to center the center line of a display screen 50 on the display apparatus and mount the driver ICs. Using the three-side free configuration, the gate driver circuit may be produced by high-temperature polysilicon technology, low-temperature polysilicon technology or the like (i.e., at least one of the source driver circuit 14 and gate driver circuit 12 may be formed directly on the array board 71 by polysilicon technology).

automatically according to input images (detection of moving pictures) or manually by the user. Alternatively, the switching can be done according to input ~~outlet~~ content such as video on the display apparatus.

Please replace the paragraph at page 137, lines 3-12, with the following rewritten paragraph:

Needless to say, the above items also apply to the pixel configurations for current programming in Figure 38 and the like as well as to the pixel configurations for voltage programming in Figures 43, 51, 54, and the like. This can be accomplished through on/off control of the transistor 11d in Figure 38, transistor 11d in Figure 43, and transistor 11e in Figure [[51]] 115. In this way, by turning on and off the wiring which delivers current to the EL elements 15, the N-fold pulse driving according to the present invention can be implemented easily.

Please replace the paragraph at page 146, lines 3-15, with the following rewritten paragraph:

Needless to say, the drive operation in ~~(c) of Figure 33(b)~~ Figures 33(b) and 33(c) may be performed after resetting all the pixels in the screen simultaneously or during scanning. Also, it goes without saying that pixel rows may be reset (at intervals of one or more pixel rows) in interlaced driving mode (scanning at intervals of one or more pixel rows). Also, pixel rows may be reset at random. The reset driving according to the present invention involves operating pixel rows (i.e., controlling the vertical direction of the screen). However, the concept of reset driving does not limit control directions to the pixel row direction. For example, it goes without saying that reset driving may be performed in the direction of pixel columns.

programming current flows through the driver transistor 11a. As can be seen From Figure 3, when a selected pixel 16 is in programming mode, the gate terminal voltage of the driver transistor 11a equals the potential of the source signal line 18.

Please replace the paragraph beginning at page 211, line 24, through page 212, line 11, with the following rewritten paragraph:

Incidentally, it has been described that a voltage resistance process in the range of 2.5-V to 10-V (both inclusive) is used for the source driver IC [[12]] 14. This voltage resistance is also applied to examples (e.g., a low-temperature polysilicon process) in which the source driver circuit 14 is formed directly on an array board 71. Working voltage resistance of a source driver circuit 14 formed directly on an array board 71 can be high and exceeds 15 V in some cases. In such cases, the power supply voltage used for the source driver circuit 14 may be substituted with the IC voltage resistance illustrated in Figure 121. Also, the source driver IC 14 may have the IC voltage resistance substituted with the power supply voltage used.

Please replace the paragraph at page 211, lines 12-20, with the following rewritten paragraph:

The area of a unit transistor 484 is correlated with the variations in its output current. Figure 122 is a graph obtained by varying the transistor width W of a unit transistor 484 with the area of the unit transistor 484 kept constant. In Figure [[121]] 122, the variation of the unit transistor 484 with a channel width W of 2 μm is taken as 1. The vertical axis of the graph represents a ~~relative proportion~~ variation rate, where the variation which occurs when the channel width W is 2 μm is taken as 1.

Please replace the paragraph at page 213, lines 1-5, with the following rewritten paragraph:

In Figure 122, the permissible limit to the variation rate is 3 for 64- to 256-gradation display. The variation rate varies with the ~~area~~ shape of the unit transistor 484. However, the variation rate with respect to ~~the IC voltage~~ the channel width W resistance is hardly affected by the ~~area~~ shape of the unit transistor 484.

Please replace the paragraph at page 214, lines 4-~~14~~ 15, with the following rewritten paragraph:

Programming current Iw is output (drawn) to the source signal line via switches controlled by 6-bit image data consisting of D0, D1, D2, ..., and D5. Thus, according to activation and deactivation of the 6-bit image data consisting of D0, D1, D2, ..., and D5, currents 1 time, 2 times, 4 times, ... and/or 32 times as large as the final-stage current source 473 are added and outputted to the output line. That is, according to activation and deactivation of the 6-bit image data consisting of D0, D1, D2, ..., and D5, 0 to 63 times as large a current as the final-stage current source 473 is output from the output line (the current is drawn from the source signal line [[18]] 18).

Please replace the paragraph at page 214, lines ~~15-19~~ 16-20, with the following rewritten paragraph:

Actually, as illustrated in ~~Figures 76, 77, 78, and 118~~ Figure 77, in the source driver IC 14, reference currents (IaR, IaG, and IaB) for R, G, and B, respectively, can be adjusted by registers 491 (491R, 491G, and 491B). By adjusting the reference currents Ia, the white balance can be adjusted easily.

Please replace the paragraph at page 234, lines ~~6-9~~ 10-14, with the following rewritten paragraph:

However, if transistors are connected in a one-to-one relationship with other transistors, any variation in the characteristics (Vt, etc.) ~~of characteristics~~ of a transistor will result in variations in the output of the corresponding transistor connected to it.

Please replace the paragraph at page 236, lines 8-12, with the following rewritten paragraph:

The use of multiple transistors for current-based delivery makes it possible to reduce variations in output current of the transistor group as a whole and further reduce variations ~~in~~ among the output current (programming current) of each terminal.

Please replace the paragraph at page 237, lines 12-22, with the following rewritten paragraph:

Now, description will be given of the relationship between the formation area of the transmission transistor group 521 and the unit transistors 484. As also illustrated in Figure [[50]] 48, a plurality of unit transistors 484 are connected per one transistor 473b. In the case of 64 gradations, 63 unit transistors 484 correspond to one transistor 473b (configuration in Figure 48). If the channel length L of the unit transistor [[473]] 484 is 10 μm and channel width W of the unit transistor 473 is 10 μm, the formation area Ts (square μm) of the unit transistor group (63 unit transistors 484, in this example) is 10 μm × 10 μm × 63 = 6300 square μm.

possible to reduce variations in output current and achieve proper image display as well as to reduce costs.

Please replace the paragraph at page 261, lines 1-7, with the following rewritten paragraph:

A regulator (electronic regulator) 491R for reference current adjustment is placed in a reference current circuit ~~654R~~ 691R for R, a regulator (electronic regulator) 491G for reference current adjustment is placed in a reference current circuit ~~654G~~ 691G for G, and a regulator (electronic regulator) 491B for reference current adjustment is placed in a reference current circuit ~~654B~~ 691B for B.

Please replace the paragraph at page 261, lines 15-19, with the following rewritten paragraph:

Output pads (output terminals) 681 are formed or placed on the output terminals of the IC chip and connected with the source signal lines 18 of the display panel. A bump is formed on the output pads 681 by a plating technique or ball bonding technique. The bump should be 10 to 40 μm high (both inclusive).

Please replace the paragraph beginning at page 265, line 20, through page 266, line 11, with the following rewritten paragraph:

Incidentally, it is also useful to vary the precharge voltage and gradation range among R, G, and B because emission start voltage and emission brightness of EL elements 15 vary among R, G, and B. For example, selective precharging is performed for 1/8 of all the gradations beginning with the 0th gradation (e.g., in the case of 64 gradations, image data is written after precharging for the ~~0th~~ 0th to 7th gradations) in the case of R. In the case of

other colors (G and B), selective precharging is performed for 1/16 of all the gradations beginning with the 0th gradation (e.g., in the case of 64 gradations, image data is written after precharging for the 0th to 3rd gradations). Regarding the precharge voltage, if 7 V is written into the source signal lines 18 for R, 7.5 V is written into the source signal lines 18 for the other colors (G and B). Optimum precharge voltage often varies with the production lot of the EL display panel. Thus, preferably precharge voltage can be adjustable with an external regulator. Such a regulator circuit can be implemented easily using an electronic regulator.

Please replace the paragraph at page 266, lines 12-14, with the following rewritten paragraph:

Incidentally, it is preferable that the precharge voltage is not higher than the anode voltage Vdd minus 0.5 V and ~~within~~ not lower than the anode voltage Vdd minus 2.5 V in Figure 1.

Please replace the paragraph at page 281, lines 8-13, with the following rewritten paragraph:

Also, as shown in Figure 57, a reference current INH is applied to the high-current source circuit portion. Basically, this current serves as a unit current, the required number of unit transistors 484 operate according to input data H0 to [[L5]] H5, and the total current flows in a ~~low-current~~ high-current portion as a programming current IwH.

Please replace the paragraph at page 284, line 12, through page 285, line 6, with the following rewritten paragraph:

Examples of the present invention are described by citing mainly the pixel configuration in Figure 1, but this is not restrictive. Needless to say, other pixel